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| EXAMINER | |
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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Paper No. 1

Application Number: 09/595,860
Filing Date: 06-16-2000
Appellant(s): Berthold et al.

Laurence A. Greenberg
For Appellant



**EXAMINER'S ANSWER**

This is in response to appellant's brief on appeal filed 01-29-2004.

***(1) Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

***(2) Related Appeals and Interferences***

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

***(3) Status of Claims***

The statement of the status of the claims contained in the brief is correct.

***(4) Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

***(5) Summary of Invention***

The summary of invention contained in the brief is correct.

***(6) Issues***

The appellant's statement of the issues in the brief is correct.

***(7) Grouping of Claims***

Claims 2-23 and 27 stand or fall with claim 1.

***(8) Claims Appealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

***(9) Prior Art of Record***

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

| | | |
|---|---|---|
| 5,552,627 | McCollum et al. | 09-1996 |
| 5,679,269 | Cohen et al. | 10-1997 |
| 5,739,579 | Chiang et al. | 04-1998 |
| 5,798,559 | Bothra et al. | 1998 |
| 5,935,766 | Cheek et al. | 08-1999 |
| 6,008,117 | Hong et al. | 12-19999 |

***(10) Grounds of Rejection***

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC ' 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 18-23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. (US 5,935,766) in view of Cohen et al. (US 5,679,269) and further in view of Bothra et al. (US 5,798,559).

Regarding claims 1, 3- 6, Cheek et al. discloses an integrated circuit comprising: a plurality of structure planes on which the metalizations are formed; the structure planes including an element structure plane (a substrate 100); electrically active elements formed on the element structure plane; a first insulation layer (130, a semiconductor oxide layer. Col.6 lines 12-19) formed above the element structure plane, the first insulation layer having first contact holes filled with a metal (140, 142, 144); a second insulation layer (160) formed above the first insulation layer, the second insulation layer having second contact holes and filled with tungsten electrical connecting leads ( 190, 192, 194) (col.7 lines 5-15); connection pieces ( Al metal-1 layers 150, 152, 154. Col.6, lines 35-40) formed underneath the electrical connecting leads and covering the first contact holes and contacting the connection leads; the connection pieces are covered by the second insolation layer (160). See Cheek et al.'s Fig.1N.

Cheek et al. does not teach that at least one diffusion blocker layer formed between first and second insulation layers and underneath the electrical connecting leads, wherein the diffusion blocker is interrupted only in a region having first contact holes and the connection pieces covering the contact hole. Cheek et al. also does not teach that the second contact holes are filled with copper in a whole-area manner.

Cohen et al. discloses an integrated circuit comprising: a contact hole (45) is filled with tungsten or Cu (col.6, lines 10-15) in a whole-area manner. See Cohen.'s Fig.3.

Bothra et al. discloses an integrated circuit comprising: a silicon nitride diffusion blocker layer (116) (col.4 lines 50-55) formed between first and second insulation layers and underneath electrical connecting lead (134), wherein the diffusion blocker is interrupted only in a region having first contact holes (114, 110) and connection pieces (118) covering the contact hole. See Bothra et al.'s Fig.3K.

It would have been obvious to one of ordinary skill in the art to fill the second contact holes of Cu instead of W as taught by Cohen et al. in Cheek et al.'s device because Cu and W are art recognized material for filling the contact holes in the semiconductor integrated circuit and they are interchangeable. It also would have been obvious to one of ordinary skill in the art to incorporate the silicon nitride blocker layer as taught by Bothra et al. into Cheek et al.'s device in order to prevent the moisture that cause corrosion or contaminants to reach the semiconductor substrate. See Bothra et al.'s col.4 lines 52-60.

It is noted that the diffusion blocker layer is formed of silicon nitride which is the same as material for forming the diffusion blocker layer in the present invention. So, it is

inherent that the diffusion blocker layer in prior art will impede and prevent diffusion of copper as claimed.

Regarding claims 2, 18, 19, 20, Cheek et al. further teaches that a Ti/TiN layer (a further diffusion blocker) is formed on a surface second contact holes (col.7 lines 5-15). It is inherent that, when the second contact holes are filled with Cu, the Ti/TiN layer will function as a diffusion barrier layer impeding the diffusion of Cu in the second contact holes into the second insulating layer.

Regarding claim 27, when the device of Cheek et al. as modified by , Cohen et al. and Bothra et al. is formed, the blocker layer inherently includes an upper surface facing the second insulation layer and a lower surface facing the structure plane and connection pieces would be in contact with the upper surface of the blocker layer.

Regarding claim 7, Bothra et al. discloses silicon nitride blocker which has the the chemical formula Si3N4.

Regarding claims 21-23, Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above. However, these references do not teach that the blocker layer has a thickness greater than a thickness of the further blocker so that a diffusion through the blocker layer is less than 10% of a diffusion through the further diffusion blocker.

One of ordinary skill would readily conclude from the art as presently combined that the diffusion through the blocker layer is dependent on the thickness of the blocker.

Therefore, it would have been prima facie obvious to one of ordinary skill in the art to form the blocker layer having a thickness greater than the thickness of further

blocker layer so that the diffusion through the blocker layer is minimal compared to diffusion through the further diffusion blocker as claimed because the thickness of blocker layers is art recognized variable of importance which is subject to routine experimentation and optimization. Appellants have failed to ascribe any criticality or adducibly vitiate the prima facie obviousness of the recited thickness.

Claims 8, 9, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Chiang et al. (US 5,739,579).

Regarding claims 8, 9, Cheek et al., Cohen et al. and Bothra et al. teach substantially all the limitations. However, Bothra et al. does not teach that the blocker layer is formed of SiON.

It is taught by Chiang et al. that SiN and SiON are art recognized material for forming the blocker layer (etch-stop layer) in an integrated circuit and they are interchangeable. See Chiang et al.'s col.14, lines 65-67.

Therefore, it would have been obvious to one of ordinary skill in the art to form the blocker layer of SiON instead of SiN as taught by Chiang et al.

Regarding claim 14, Cheek et al., Cohen et al. and Bothra et al. teach substantially all the limitations. However, Bothra et al. does not teach that the blocker layer has a thickness of between 50 nm and 800 nm.

Chiang et al. further teach that the silicon nitride diffusion blocker layers (323) have a thickness in the range of 30 nm to 150 nm (Chiang et al.'s col.15, lines 17-22). See Chiang et al.'s Fig.25.

It would have been obvious to one of ordinary skill in the art to provide a blocker layer having the thickness as taught by Chiang et al. because the thickness of the blocker layer is an art recognized variable of importance which is subject to routine experimentation and optimization.

Regarding claims 15 and 16, Cheek et al., Cohen et al. and Bothra et al. teach substantially all the limitations. However, these references do not teach that blocker layers are disposed on different ones of structure planes.

Chiang et al. further teaches that the silicon nitride diffusion blocker layers (323, 390, 392) are formed between each of a plurality of structure planes. See Chiang et al.'s Fig.25.

It would have been obvious to one of ordinary skill in the art to incorporate the silicon nitride blocker layers between the structure planes as taught by Chiang et al. into Cheek et al.'s device in order to prevent electrical shorting. Chiang et al..'s col.15, lines 4-15.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Hong (US 6,008,117).

Cheek et al., Cohen et al. and Bothra et al. teach substantially all the limitations but fail to teach that the blocker layer is formed of metal oxide such as TiO2.

Hong discloses an integrated circuit comprising a blocker layer (14) formed of silicon nitride or TiO2. See Hong's Fig.1H and col.2 lines 52-56.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of TiO2 instead of silicon nitride as taught by Hong because materials such as silicon nitride, and TiO2 are art recognized materials for forming the blocker layer in the semiconductor device and they are interchangeable.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of McCollum et al. (US 5,552,627).

Cheek et al., Cohen et al. and Bothra et al. teach substantially all the limitations but fail to teach that the blocker layer is formed of a fluorinated nitride such as fluorooxynitride.

McCollum et al. discloses an integrated circuit comprising a blocker layer formed of fluorinated nitride material by depositing the silicon nitride using an NF3 atmosphere in the reactor. McCollum et al. teaches that fluorinated nitride has a lower leakage than other nitride material. See McCollum et al.'s Fig.3 and col.8, lines 42-51.

Therefore, it would have been obvious to one of ordinary skill in the art to form the block layer of silicon nitride or silicon oxynitride by depositing the silicon nitride using an NF3 atmosphere as taught by McCollum et al. in order to reduce the leakage of the blocker layer.

The claimed fluorinated nitride such as fluorooxynitride would inherently result in the process of McCollum because the silicon nitride is deposited in an NF3 atmosphere.

***(11) Response to Argument***

Appellants argue that the purpose of silicon nitride layer (116) in Bothra et al. is different from the diffusion layer (160) in present disclosure. In response, as above discussed, the diffusion blocker layer in the device that would have been obvious from Cheek et al., Cohen et al. and Bothra et al. is formed of silicon nitride which is materially identical to the diffusion blocker layer in the present claim 7. Therefore the diffusion blocker layer of the prior art device would inherently prevent a copper diffusion as claimed. It is noted that, if it is obvious to combine references for one reason it is obvious to combine references for all reasons. In re Grap, 145 USPQ 197 (CCPA 1965); In re Finsterwalder, 168 USPQ 1970); In re Kronig, 539 F.2d 1300, 190 USPQ 425 (CCPA 1976). In re Dillon, 892 F .2d 1544, 13 USPQ 1337 (1989); In re Dillon 919 F.2d 688, 16 USPQ 1897 Fed. Cir. 1990).

Appellants argue that the Examiner did not point to anywhere in the cited reference (Bothra et al.'s reference) that provides a reason to combine the diffusion blocker into Cheek et al.'s reference. In response, as above discussed, Bothra et al. teaches that a silicon nitride diffusion blocker layer (116) (col.4 lines 50-55) formed between first and second insulation layers and underneath electrical connecting lead (134), wherein the diffusion blocker is interrupted only in a region having first contact holes (114, 110) and connection pieces (118) covering the contact hole (Fig.3K) in order to prevent the moisture that cause corrosion or contaminants to reach the semiconductor substrate (col.4 lines 52-60). For these reasons alone, one of ordinary skill in the art would be motivated to incorporate the diffusion blocker of Bothra into Cheek et al.'s device.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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4/15/04

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